WHAT IS CLAIMED IS:

1. A method of manufacturing a liquid crystal display device, comprising:

forming a gate line, a gate pad and a gate electrode on a first substrate through a first mask process;

forming a data line, a data pad, a source electrode, a drain electrode and an active layer on the first substrate including the gate line, the gate pad and the gate electrode through a second mask process; forming a pixel electrode and a data pad terminal on the first substrate including the data line, the data pad, the source electrode and the drain electrode through a third mask process;

forming a passivation layer on an entire surface of the first substrate including the pixel electrode and the data pad terminal;

attaching the first substrate including the passivation layer with a second substrate, wherein a gate pad portion including the gate pad and a data pad portion including the data pad are exposed by the second substrate;

providing a liquid crystal material into a gap between the first and second substrates; and removing the passivation layer in the gate and data pad portions exposed by the second substrate.

2. The method of claim 1, wherein providing a liquid material includes injecting the liquid crystal material.

3. The method of claim 1, wherein providing a liquid crystal material includes applying the liquid crystal material.

4. The method according to claim 1, wherein removing the passivation layer in the gate and data pad portions includes dipping the liquid crystal display device into an etchant.

5. The method according to claim 4, wherein the passivation layer is made of one of silicon nitride and silicon oxide.

6. The method according to claim 5, wherein the etchant includes fluoride acid (HF).

7. The method according to claim 1, wherein the second mask process includes:

forming a gate insulating layer on the first substrate including the gate line, the gate electrode and the gate pad;

depositing an amorphous silicon layer, a doped amorphous silicon layer and a metal layer over the gate insulating layer;

providing a photoresist pattern having first and second thicknesses over the second metal layer, wherein the second thickness is smaller than the first thickness;

selectively removing portions of the metal layer, the doped amorphous silicon layer and the amorphous silicon layer according to the photoresist pattern;

removing a portion of the photoresist pattern having the second thickness;

selectively etching the metal layer exposed by removing the portion of the photoresist pattern having the second thickness; and

removing the remaining photoresist pattern.

8. The method according to claim 7, wherein the third mask process includes selectively etching the doped amorphous silicon layer exposed by the selective etching of the metal layer exposed by removing the photoresist pattern having the second thickness.

9. The method according to claim 7, wherein the second mask process further includes selectively removing the gate insulating layer.

10. The method according to claim 1, wherein the third mask process includes forming a data buffer pattern covering the data line and the source electrode.

11. The method according to claim 1, wherein the gate line, the gate electrode and the gate pad include aluminum.

12. The method according to claim 11, wherein the gate line, the gate electrode and the gate pad further include a transparent conductive material layer.

13. The method according to claim 1, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the data line and the data pad.

14. The method according to claim 1, wherein the second mask process includes a a capacitor electrode over the gate line.

15. The method according to claim 14, wherein the pixel electrode contacts the capacitor electrode, whereby the capacitor electrode forms a storage capacitor with the gate line.

16. The method according to claim 14, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the capacitor electrode.

17. The method according to claim 1, wherein the second mask process further includes a gate pad buffer pattern over the gate pad, the gate pad buffer pattern including a hole corresponding to a middle portion of the gate pad.

18. The method according to claim 17, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the gate pad buffer pattern.

19. The method according to claim 17, wherein the third mask process further includes a gate pad terminal connected to the gate pad through the hole corresponding to the middle portion of the gate pad.

20. The method according to claim 1, wherein the second mask process uses a slit mask.

21. The method according to claim 1, wherein the second mask process uses a halftone mask.

22. A method of manufacturing a liquid crystal display device, comprising:

forming a gate line, a gate pad and a gate electrode on a first substrate through a first mask process;

forming a data line, a data pad, a source/drain pattern and an active layer on the first substrate including the gate line, the gate pad and the gate electrode through a second mask process;

forming a pixel electrode, a data buffer pattern and a data pad terminal on the first substrate including the data line, the data pad, the source/drain pattern through a third mask process, and patterning the source/drain pattern by using the pixel electrode and the data buffer pattern as a mask, thereby forming a source electrode and a drain electrode;

forming a passivation layer on an entire surface of the first substrate including the pixel electrode, the data buffer pattern and the data pad terminal;

attaching the first substrate including the passivation layer with a second substrate, wherein a gate pad portion including the gate pad and a data pad portion including the data pad are exposed by the second substrate;

providing a liquid crystal material into a gap between the first and second substrates; and

removing the passivation layer in the gate and pad portions exposed by the second substrate.

23. The method according to claim 21, wherein providing a liquid crystal material includes one of injecting and applying the liquid crystal material.

24. The method according to claim 22, wherein removing the passivation layer in the gate and data pad portions includes dipping the liquid crystal display device into an etchant.

25. The method according to claim 24, wherein the passivation layer is made of one of silicon nitride and silicon oxide.

26. The method according to claim 25, wherein the etchant includes fluoride acid (HF).

27. The method according to claim 22, wherein the second mask process includes:

forming a gate insulating layer on the first substrate including the gate line, the gate electrode and the gate pad;

depositing an amorphous silicon layer, a doped amorphous silicon layer and a metal layer over the gate insulating layer;

providing a photoresist pattern over the metal layer;

selectively removing portions of the metal layer, the doped amorphous silicon layer and the amorphous silicon layer according to the photoresist pattern; and

removing the remaining photoresist pattern.

28. The method according to claim 27, wherein the third mask process includes selectively etching the doped amorphous silicon layer using the source and drain electrodes as a mask.

29. The method according to claim 27, wherein the second mask process further includes a step of selectively removing the gate insulating layer.

30. The method according to claim 22, wherein the gate line, the gate electrode and the gate pad include aluminum.

31. The method according to claim 30, wherein the gate line, the gate electrode and the gate pad further include a transparent conductive material layer.

32. The method according to claim 22, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the data line and the data pad.

33. The method according to claim 22, wherein the second mask process includes a capacitor electrode over the gate line.

34. The method according to claim 33, wherein the pixel electrode contacts the capacitor electrode, whereby the capacitor electrode forms a storage capacitor with the gate line.

35. The method according to claim 33, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the capacitor electrode.

36. The method according to claim 33, wherein the second mask process further includes forming a gate pad buffer pattern over the gate pad, the gate pad buffer pattern including a hole corresponding to a middle portion of the gate pad.

37. The method according to claim 36, wherein an amorphous silicon layer and a doped amorphous silicon layer are formed under the gate pad buffer pattern.

38. The method according to claim 36, wherein the third mask process further includes forming a gate pad terminal connected to the gate pad through the hole corresponding to the middle portion of the gate pad.